

WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#)[Search Form](#)[Posting Counts](#)[Show S Numbers](#)[Edit S Numbers](#)[Preferences](#)[Cases](#)**Search Results -**

| Term | Documents |
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| (1 AND 12).USPT. | 61 |
| (L1 AND L12).USPT. | 61 |

Database:

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| US Patents Full-Text Database | ▲ |
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| JPO Abstracts Database | |
| EPO Abstracts Database | |
| Derwent World Patents Index | |
| IBM Technical Disclosure Bulletins | ▼ |

Search:

L13

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History****DATE:** Saturday, December 06, 2003 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=OR*L13 l1 and L1261 L13L12 L11 and pipelin\$55192 L12L11 L10 or l816324 L11L10 ((712/23)!.CCLS.)630 L10L9 l1 and L899 L9L8 l2 or L716221 L8

L7 ((711/123 |711/124 |711/125 |711/126 |711/127 |711/128 |711/129
 |711/130 |711/131 |711/132 |711/133 |711/134 |711/135 |711/136
 |711/137 |711/138 |711/139 |711/140 |711/141 |711/142 |711/143
 |711/144 |711/145 |711/146 |711/147 |711/148 |711/149 |711/150
 |711/151 |711/152 |711/153 |711/154 |711/155 |711/156 |711/157
 |711/158 |711/159 |711/160 |711/161 |711/162 |711/163 |711/164
 |711/165 |711/166 |711/167 |711/168 |711/169 |711/170 |711/171
 |711/172 |711/173 |711/200 |711/201 |711/202 |711/203 |711/204
 |711/205 |711/206 |711/207 |711/208 |711/209 |711/210 |711/211
 |711/212 |711/213 |711/214 |711/215 |711/216 |711/217 |711/218
 |711/219 |711/220 |711/221)!.CCLS.)

11697 L7*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*L6 (711/123-173)!0 L6L5 (711/123-221)!0 L5L4 (711/123-221)!0 L4L3 (711-123-221)!0 L3*DB=USPT; PLUR=YES; OP=OR*

L2 ((712/205 |712/206 |712/207 |712/208 |712/209 |712/210 |712/211
 |712/212 |712/213 |712/214 |712/215 |712/216 |712/217 |712/218
 |712/219 |712/220 |712/221 |712/222 |712/223 |712/224 |712/225
 |712/226 |712/227 |712/228 |712/229 |712/230 |712/231 |712/232
 |712/233 |712/234 |712/235 |712/236 |712/237 |712/238 |712/239
 |712/240 |712/241 |712/242 |712/243 |712/244 |712/245 |712/246
 |712/247 |712/248)!.CCLS.)

5297 L2*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*L1 (bypass\$3 or eliminat\$3 or repeat\$3 or avoid\$3) near5 address\$3
near5 (comput\$3 or calculat\$5)526 L1

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 20 of 61 returned.**☐ 1. Document ID: US 6625719 B2

L13: Entry 1 of 61

File: USPT

Sep 23, 2003

US-PAT-NO: 6625719

DOCUMENT-IDENTIFIER: US 6625719 B2

TITLE: Processing devices with improved addressing capabilities systems and methods

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 2. Document ID: US 6611885 B2

L13: Entry 2 of 61

File: USPT

Aug 26, 2003

US-PAT-NO: 6611885

DOCUMENT-IDENTIFIER: US 6611885 B2

TITLE: Method and apparatus for synchronous data transfers in a memory device with selectable data or address paths

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 3. Document ID: US 6571318 B1

L13: Entry 3 of 61

File: USPT

May 27, 2003

US-PAT-NO: 6571318

DOCUMENT-IDENTIFIER: US 6571318 B1

TITLE: Stride based prefetcher with confidence counter and dynamic prefetch-ahead mechanism

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 4. Document ID: US 6560697 B2

L13: Entry 4 of 61

File: USPT

May 6, 2003

US-PAT-NO: 6560697

DOCUMENT-IDENTIFIER: US 6560697 B2

TITLE: Data processor having repeat instruction processing using executed instruction number counter

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 5. Document ID: US 6560668 B2

L13: Entry 5 of 61

File: USPT

May 6, 2003

US-PAT-NO: 6560668

DOCUMENT-IDENTIFIER: US 6560668 B2

TITLE: Method and apparatus for reading write-modified read data in memory device providing synchronous data transfers

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 6. Document ID: US 6556483 B2

L13: Entry 6 of 61

File: USPT

Apr 29, 2003

US-PAT-NO: 6556483

DOCUMENT-IDENTIFIER: US 6556483 B2

TITLE: Method and apparatus for synchronous data transfers in a memory device with selectable data or address paths

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|
| Draw Desc | Image | | | | | | | | | | |

☐ 7. Document ID: US 6553474 B2

L13: Entry 7 of 61

File: USPT

Apr 22, 2003

US-PAT-NO: 6553474

DOCUMENT-IDENTIFIER: US 6553474 B2

TITLE: Data processor changing an alignment of loaded data

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KMC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|-----|
| Draw Desc | Image | | | | | | | | | |

☐ 8. Document ID: US 6526502 B1

L13: Entry 8 of 61

File: USPT

Feb 25, 2003

US-PAT-NO: 6526502

DOCUMENT-IDENTIFIER: US 6526502 B1

TITLE: Apparatus and method for speculatively updating global branch history with branch prediction prior to resolution of branch outcome

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMC

☐ 9. Document ID: US 6484253 B1

L13: Entry 9 of 61

File: USPT

Nov 19, 2002

US-PAT-NO: 6484253

DOCUMENT-IDENTIFIER: US 6484253 B1

TITLE: Data processor

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMC

☐ 10. Document ID: US 6421771 B1

L13: Entry 10 of 61

File: USPT

Jul 16, 2002

US-PAT-NO: 6421771

DOCUMENT-IDENTIFIER: US 6421771 B1

TITLE: Processor performing parallel operations subject to operand register interference using operand history storage

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMC

☐ 11. Document ID: US 6415340 B1

L13: Entry 11 of 61

File: USPT

Jul 2, 2002

US-PAT-NO: 6415340

DOCUMENT-IDENTIFIER: US 6415340 B1

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for synchronous data transfers in a memory device with selectable data or address paths

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMC

☐ 12. Document ID: US 6397316 B2

L13: Entry 12 of 61

File: USPT

May 28, 2002

US-PAT-NO: 6397316

DOCUMENT-IDENTIFIER: US 6397316 B2

TITLE: System for reducing bus overhead for communication with a network interface

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 13. Document ID: US 6345357 B1

L13: Entry 13 of 61

File: USPT

Feb 5, 2002

US-PAT-NO: 6345357

DOCUMENT-IDENTIFIER: US 6345357 B1

TITLE: Versatile branch-less sequence control of instruction stream containing step repeat loop block using executed instructions number counter

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 14. Document ID: US 6308322 B1

L13: Entry 14 of 61

File: USPT

Oct 23, 2001

US-PAT-NO: 6308322

DOCUMENT-IDENTIFIER: US 6308322 B1

TITLE: Method and apparatus for reduction of indirect branch instruction overhead through use of target address hints

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 15. Document ID: US 6272608 B1

L13: Entry 15 of 61

File: USPT

Aug 7, 2001

US-PAT-NO: 6272608

DOCUMENT-IDENTIFIER: US 6272608 B1

TITLE: Method and apparatus for synchronous data transfers in a memory device with lookahead logic for detecting latency intervals

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 16. Document ID: US 6199152 B1

L13: Entry 16 of 61

File: USPT

Mar 6, 2001

US-PAT-NO: 6199152

DOCUMENT-IDENTIFIER: US 6199152 B1

TITLE: Translated memory protection apparatus for an advanced microprocessor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|------------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Drawl Desc | Image | | | | | | | | |

KVMC

☐ 17. Document ID: US 6189091 B1

L13: Entry 17 of 61

File: USPT

Feb 13, 2001

US-PAT-NO: 6189091

DOCUMENT-IDENTIFIER: US 6189091 B1

TITLE: Apparatus and method for speculatively updating global history and restoring same on branch misprediction detection

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|------------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Drawl Desc | Image | | | | | | | | |

KVMC

☐ 18. Document ID: US 6145074 A

L13: Entry 18 of 61

File: USPT

Nov 7, 2000

US-PAT-NO: 6145074

DOCUMENT-IDENTIFIER: US 6145074 A

**** See image for Certificate of Correction ****

TITLE: Selecting register or previous instruction result bypass as source operand path based on bypass specifier field in succeeding instruction

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|------------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Drawl Desc | Image | | | | | | | | |

KVMC

☐ 19. Document ID: US 6145069 A

L13: Entry 19 of 61

File: USPT

Nov 7, 2000

US-PAT-NO: 6145069

DOCUMENT-IDENTIFIER: US 6145069 A

**** See image for Certificate of Correction ****

TITLE: Parallel decompression and compression system and method for improving storage density and access speed for non-volatile memory and embedded memory devices

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|------------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Drawl Desc | Image | | | | | | | | |

KVMC

☐ 20. Document ID: US 6138230 A

L13: Entry 20 of 61

File: USPT

Oct 24, 2000

US-PAT-NO: 6138230

DOCUMENT-IDENTIFIER: US 6138230 A

TITLE: Processor with multiple execution pipelines using pipe stage state information to control independent movement of instructions between pipe stages of an execution pipeline

| | | | | | | | | | | |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw | Desc | Image | | | | | | | | |

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| (L1 AND L12).USPT. | 61 |

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L13: Entry 21 of 61

File: USPT

Aug 22, 2000

US-PAT-NO: 6108745

DOCUMENT-IDENTIFIER: US 6108745 A

TITLE: Fast and compact address bit routing scheme that supports various DRAM bank sizes and multiple interleaving schemes

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

[KWIC](#)☐ 22. Document ID: US 6073231 A

L13: Entry 22 of 61

File: USPT

Jun 6, 2000

US-PAT-NO: 6073231

DOCUMENT-IDENTIFIER: US 6073231 A

TITLE: Pipelined processor with microcontrol of register translation hardware

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

[KWIC](#)☐ 23. Document ID: US 6044455 A

L13: Entry 23 of 61

File: USPT

Mar 28, 2000

US-PAT-NO: 6044455

DOCUMENT-IDENTIFIER: US 6044455 A

TITLE: Central processing unit adapted for pipeline process

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

[KWIC](#)☐ 24. Document ID: US 6031992 A

L13: Entry 24 of 61

File: USPT

Feb 29, 2000

US-PAT-NO: 6031992

DOCUMENT-IDENTIFIER: US 6031992 A

TITLE: Combining hardware and software to provide an improved microprocessor

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 25. Document ID: US 6016543 A

L13: Entry 25 of 61

File: USPT

Jan 18, 2000

US-PAT-NO: 6016543

DOCUMENT-IDENTIFIER: US 6016543 A

TITLE: Microprocessor for controlling the conditional execution of instructions

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 26. Document ID: US 6006033 A

L13: Entry 26 of 61

File: USPT

Dec 21, 1999

US-PAT-NO: 6006033

DOCUMENT-IDENTIFIER: US 6006033 A

TITLE: Method and system for reordering the instructions of a computer program to optimize its execution

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 27. Document ID: US 5966729 A

L13: Entry 27 of 61

File: USPT

Oct 12, 1999

US-PAT-NO: 5966729

DOCUMENT-IDENTIFIER: US 5966729 A

TITLE: Snooper filter for use in multiprocessor computer systems

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image | | | | | | | | | |

☐ 28. Document ID: US 5958061 A

L13: Entry 28 of 61

File: USPT

Sep 28, 1999

US-PAT-NO: 5958061

DOCUMENT-IDENTIFIER: US 5958061 A

TITLE: Host microprocessor with apparatus for temporarily holding target processor state

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMMC

☐ 29. Document ID: US 5926832 A

L13: Entry 29 of 61

File: USPT

Jul 20, 1999

US-PAT-NO: 5926832

DOCUMENT-IDENTIFIER: US 5926832 A

TITLE: Method and apparatus for aliasing memory data in an advanced microprocessor

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMMC

☐ 30. Document ID: US 5924114 A

L13: Entry 30 of 61

File: USPT

Jul 13, 1999

US-PAT-NO: 5924114

DOCUMENT-IDENTIFIER: US 5924114 A

TITLE: Circular buffer with two different step sizes

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMMC

☐ 31. Document ID: US 5914727 A

L13: Entry 31 of 61

File: USPT

Jun 22, 1999

US-PAT-NO: 5914727

DOCUMENT-IDENTIFIER: US 5914727 A

TITLE: Valid flag for disabling allocation of accelerated graphics port memory space

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMMC

☐ 32. Document ID: US 5901301 A

L13: Entry 32 of 61

File: USPT

May 4, 1999

US-PAT-NO: 5901301

DOCUMENT-IDENTIFIER: US 5901301 A

**** See image for Certificate of Correction ****

TITLE: Data processor and method of processing data

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMIC

☐ 33. Document ID: US 5860151 A

L13: Entry 33 of 61

File: USPT

Jan 12, 1999

US-PAT-NO: 5860151

DOCUMENT-IDENTIFIER: US 5860151 A

**** See image for Certificate of Correction ****

TITLE: Data cache fast address calculation system and method

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMIC

☐ 34. Document ID: US 5832205 A

L13: Entry 34 of 61

File: USPT

Nov 3, 1998

US-PAT-NO: 5832205

DOCUMENT-IDENTIFIER: US 5832205 A

TITLE: Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMIC

☐ 35. Document ID: US 5809309 A

L13: Entry 35 of 61

File: USPT

Sep 15, 1998

US-PAT-NO: 5809309

DOCUMENT-IDENTIFIER: US 5809309 A

TITLE: Processing devices with look-ahead instruction systems and methods

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

KMIC

☐ 36. Document ID: US 5787483 A

L13: Entry 36 of 61

File: USPT

Jul 28, 1998

US-PAT-NO: 5787483

DOCUMENT-IDENTIFIER: US 5787483 A

TITLE: High-speed data communications modem

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KVMC

☐ 37. Document ID: US 5751991 A

L13: Entry 37 of 61

File: USPT

May 12, 1998

US-PAT-NO: 5751991

DOCUMENT-IDENTIFIER: US 5751991 A

TITLE: Processing devices with improved addressing capabilities, systems and methods

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KVMC

☐ 38. Document ID: US 5724563 A

L13: Entry 38 of 61

File: USPT

Mar 3, 1998

US-PAT-NO: 5724563

DOCUMENT-IDENTIFIER: US 5724563 A

TITLE: Pipeline processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KVMC

☐ 39. Document ID: US 5717946 A

L13: Entry 39 of 61

File: USPT

Feb 10, 1998

US-PAT-NO: 5717946

DOCUMENT-IDENTIFIER: US 5717946 A

TITLE: Data processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KVMC

☐ 40. Document ID: US 5657486 A

L13: Entry 40 of 61

File: USPT

Aug 12, 1997

US-PAT-NO: 5657486

DOCUMENT-IDENTIFIER: US 5657486 A

TITLE: Automatic test equipment with pipelined sequencer

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KVMC

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L13: Entry 41 of 61

File: USPT

May 13, 1997

US-PAT-NO: 5630149

DOCUMENT-IDENTIFIER: US 5630149 A

TITLE: Pipelined processor with register renaming hardware to accommodate multiple size registers

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KVMC |
| Draw Desc | Image | | | | | | | | | |

☐ 42. Document ID: US 5596760 A

L13: Entry 42 of 61

File: USPT

Jan 21, 1997

US-PAT-NO: 5596760

DOCUMENT-IDENTIFIER: US 5596760 A

**** See image for Certificate of Correction ****

TITLE: Program control method and program control apparatus

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KVMC |
| Draw Desc | Image | | | | | | | | | |

☐ 43. Document ID: US 5535348 A

L13: Entry 43 of 61

File: USPT

Jul 9, 1996

US-PAT-NO: 5535348

DOCUMENT-IDENTIFIER: US 5535348 A

TITLE: Block instruction

| | | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KVMC |
| Draw Desc | Image | | | | | | | | | |

☐ 44. Document ID: US 5481685 A

L13: Entry 44 of 61

File: USPT

Jan 2, 1996

US-PAT-NO: 5481685

DOCUMENT-IDENTIFIER: US 5481685 A

TITLE: RISC microprocessor architecture implementing fast trap and exception state

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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/MC

☐ 45. Document ID: US 5467459 A

L13: Entry 45 of 61

File: USPT

Nov 14, 1995

US-PAT-NO: 5467459

DOCUMENT-IDENTIFIER: US 5467459 A

**** See image for Certificate of Correction ****

TITLE: Imaging and graphics processing system

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/MC

☐ 46. Document ID: US 5454089 A

L13: Entry 46 of 61

File: USPT

Sep 26, 1995

US-PAT-NO: 5454089

DOCUMENT-IDENTIFIER: US 5454089 A

**** See image for Certificate of Correction ****TITLE: Branch look ahead adder for use in an instruction pipeline sequencer with multiple instruction decoding

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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/MC

☐ 47. Document ID: US 5448705 A

L13: Entry 47 of 61

File: USPT

Sep 5, 1995

US-PAT-NO: 5448705

DOCUMENT-IDENTIFIER: US 5448705 A

TITLE: RISC microprocessor architecture implementing fast trap and exception state

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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/MC

☐ 48. Document ID: US 5432918 A

L13: Entry 48 of 61

File: USPT

Jul 11, 1995

US-PAT-NO: 5432918

DOCUMENT-IDENTIFIER: US 5432918 A

TITLE: Method and apparatus for ordering read and write operations using conflict bits in a write queue

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Draw Desc | Image | | | | | | | | | |

☐ 49. Document ID: US 5428754 A

L13: Entry 49 of 61

File: USPT

Jun 27, 1995

US-PAT-NO: 5428754

DOCUMENT-IDENTIFIER: US 5428754 A

TITLE: Computer system with clock shared between processors executing separate instruction streams

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Draw Desc | Image | | | | | | | | | |

☐ 50. Document ID: US 5390304 A

L13: Entry 50 of 61

File: USPT

Feb 14, 1995

US-PAT-NO: 5390304

DOCUMENT-IDENTIFIER: US 5390304 A

TITLE: Method and apparatus for processing block instructions in a data processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Draw Desc | Image | | | | | | | | | |

☐ 51. Document ID: US 5333288 A

L13: Entry 51 of 61

File: USPT

Jul 26, 1994

US-PAT-NO: 5333288

DOCUMENT-IDENTIFIER: US 5333288 A

TITLE: Effective address pre-calculation type pipelined microprocessor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|------|
| Draw Desc | Image | | | | | | | | | |

☐ 52. Document ID: US 5329630 A

L13: Entry 52 of 61

File: USPT

Jul 12, 1994

US-PAT-NO: 5329630

DOCUMENT-IDENTIFIER: US 5329630 A

TITLE: System and method using double-buffer preview mode

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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/M/C

☐ 53. Document ID: US 5148538 A

L13: Entry 53 of 61

File: USPT

Sep 15, 1992

US-PAT-NO: 5148538

DOCUMENT-IDENTIFIER: US 5148538 A

TITLE: Translation look ahead based cache access

| | | | | | | | | | |
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| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/M/C

☐ 54. Document ID: US 5148529 A

L13: Entry 54 of 61

File: USPT

Sep 15, 1992

US-PAT-NO: 5148529

DOCUMENT-IDENTIFIER: US 5148529 A

TITLE: Pipelined multi-stage data processor including an operand bypass mechanism

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|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/M/C

☐ 55. Document ID: US 5029070 A

L13: Entry 55 of 61

File: USPT

Jul 2, 1991

US-PAT-NO: 5029070

DOCUMENT-IDENTIFIER: US 5029070 A

TITLE: Coherent cache structures and methods

| | | | | | | | | | |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
| Draw Desc | Image | | | | | | | | |

K/M/C

☐ 56. Document ID: US 4794524 A

L13: Entry 56 of 61

File: USPT

Dec 27, 1988

US-PAT-NO: 4794524

DOCUMENT-IDENTIFIER: US 4794524 A

**** See image for Certificate of Correction ****TITLE: Pipelined single chip microprocessor having on-chip cache and on-chip memory management unit

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KMC

☐ 57. Document ID: US 4777594 A

L13: Entry 57 of 61

File: USPT

Oct 11, 1988

US-PAT-NO: 4777594

DOCUMENT-IDENTIFIER: US 4777594 A

TITLE: Data processing apparatus and method employing instruction flow prediction

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KMC

☐ 58. Document ID: US 4760519 A

L13: Entry 58 of 61

File: USPT

Jul 26, 1988

US-PAT-NO: 4760519

DOCUMENT-IDENTIFIER: US 4760519 A

TITLE: Data processing apparatus and method employing collision detection and prediction

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KMC

☐ 59. Document ID: US 4750112 A

L13: Entry 59 of 61

File: USPT

Jun 7, 1988

US-PAT-NO: 4750112

DOCUMENT-IDENTIFIER: US 4750112 A

TITLE: Data processing apparatus and method employing instruction pipelining

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KMC

☐ 60. Document ID: US 4713750 A

L13: Entry 60 of 61

File: USPT

Dec 15, 1987

US-PAT-NO: 4713750

DOCUMENT-IDENTIFIER: US 4713750 A

TITLE: Microprocessor with compact mapped programmable logic array

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
|-----------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|
| Draw Desc | Image | | | | | | | | |

KMC

| Term | Documents |
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| (1 AND 12).USPT. | 61 |
| (L1 AND L12).USPT. | 61 |

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